Figure 1

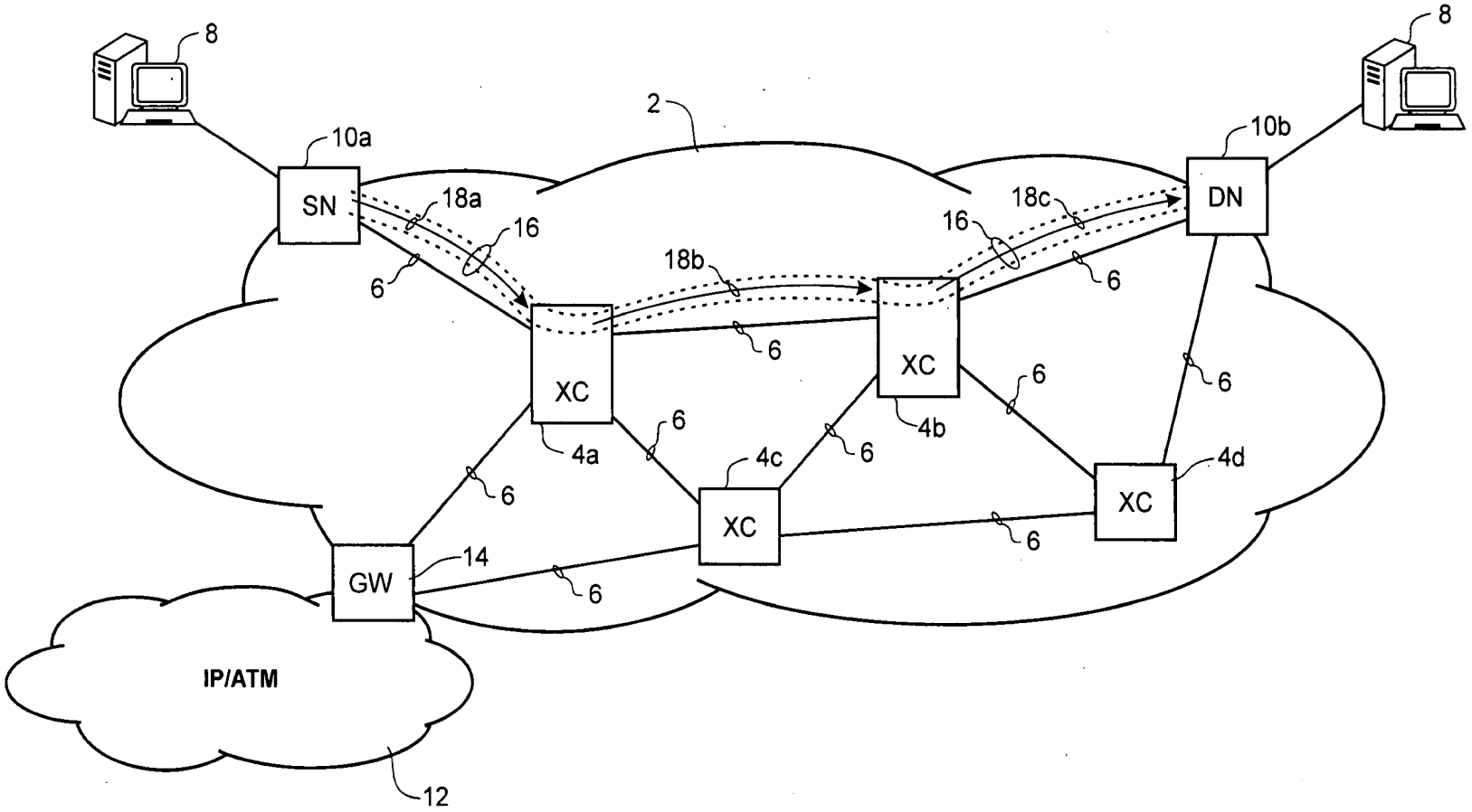
8
8
2
10a
10b
SN
DN
18a
16
18b
18c
16
6
6
6
6
6
6
6
6
6
6
6
XC
XC
XC
4a
4b
4c
4d
GW
14
IP/ATM
12

Figure 2

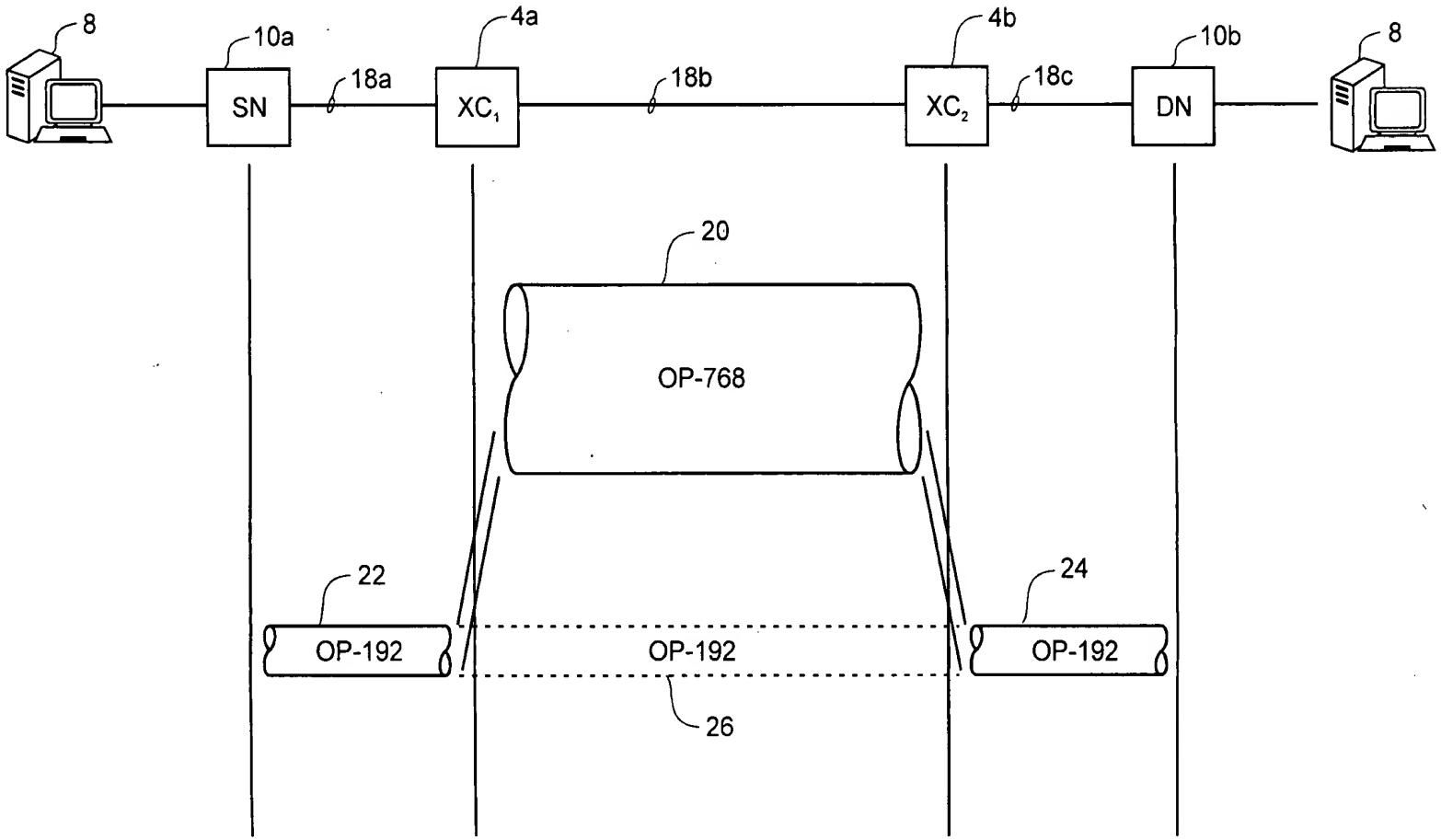
8
10a
SN
18a
4a
XC1
18b
4b
XC2
18c
10b
DN
8
20
OP-768
22
OP-192
OP-192
24
OP-192
26

Figure 3

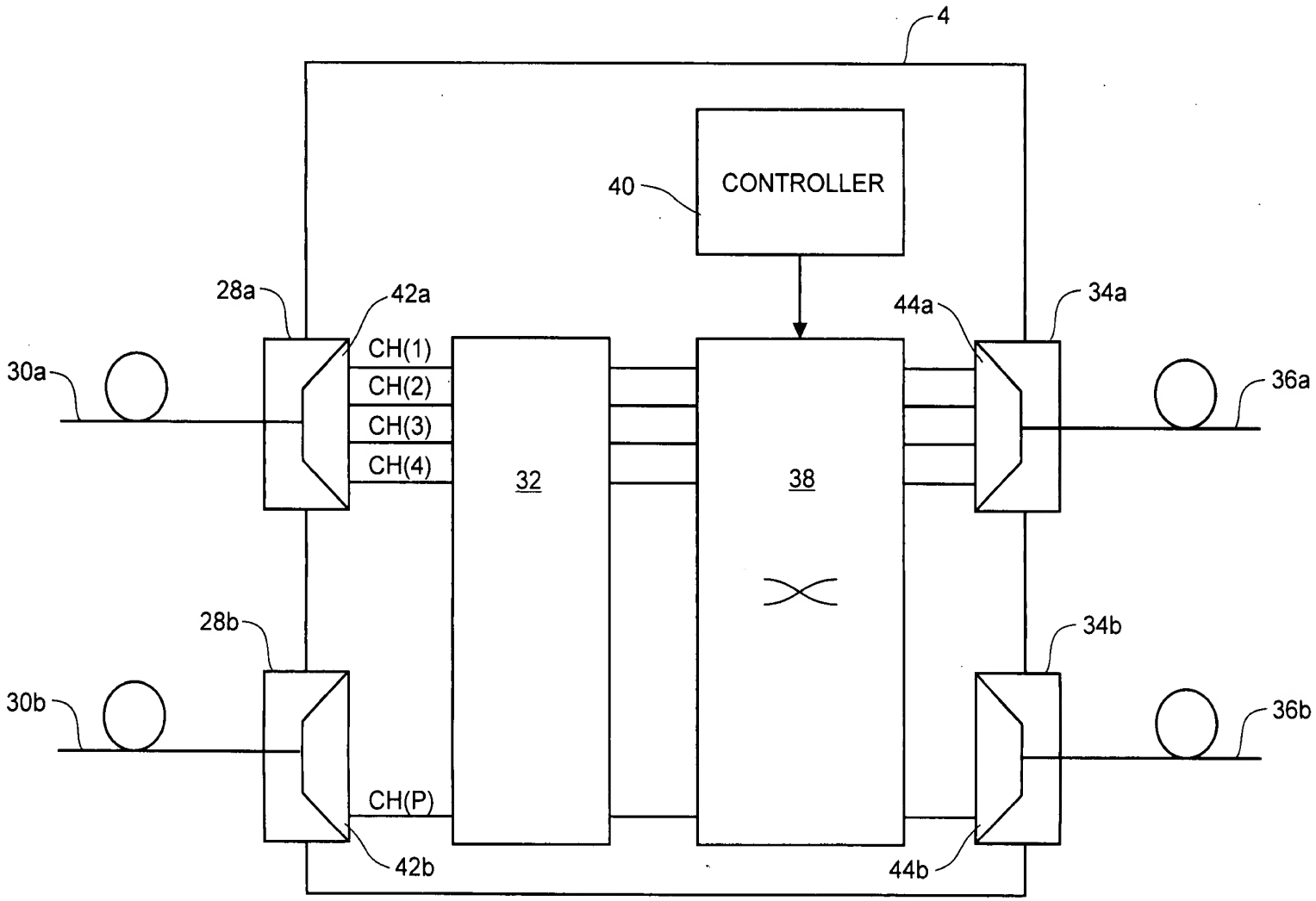
4
CONTROLLER
40
28a
42a
44a
34a
30a
CH(1)
CH(2)
CH(3)
CH(4)
32
38
36a
28b
34b
30b
36b
CH(P)
42b
44b

Figure 4

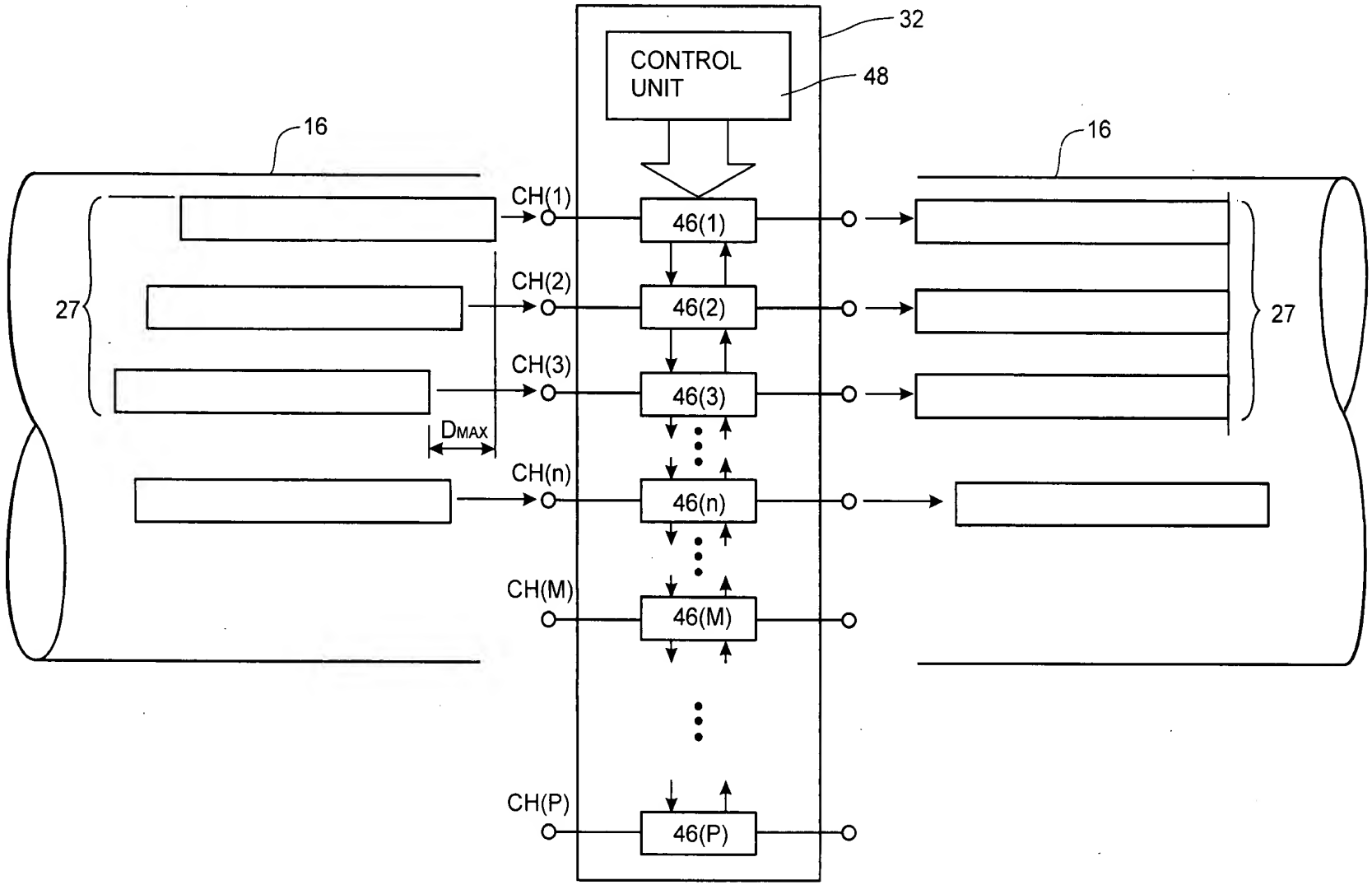
32
CONTROL UNIT
48
16
16
CH(1)
CH(2)
CH(3)
CH(n)
CH(M)
CH(P)
46(1)
46(2)
46(3)
46(n)
46(M)
46(P)
27
27
DMAX

Figure 5

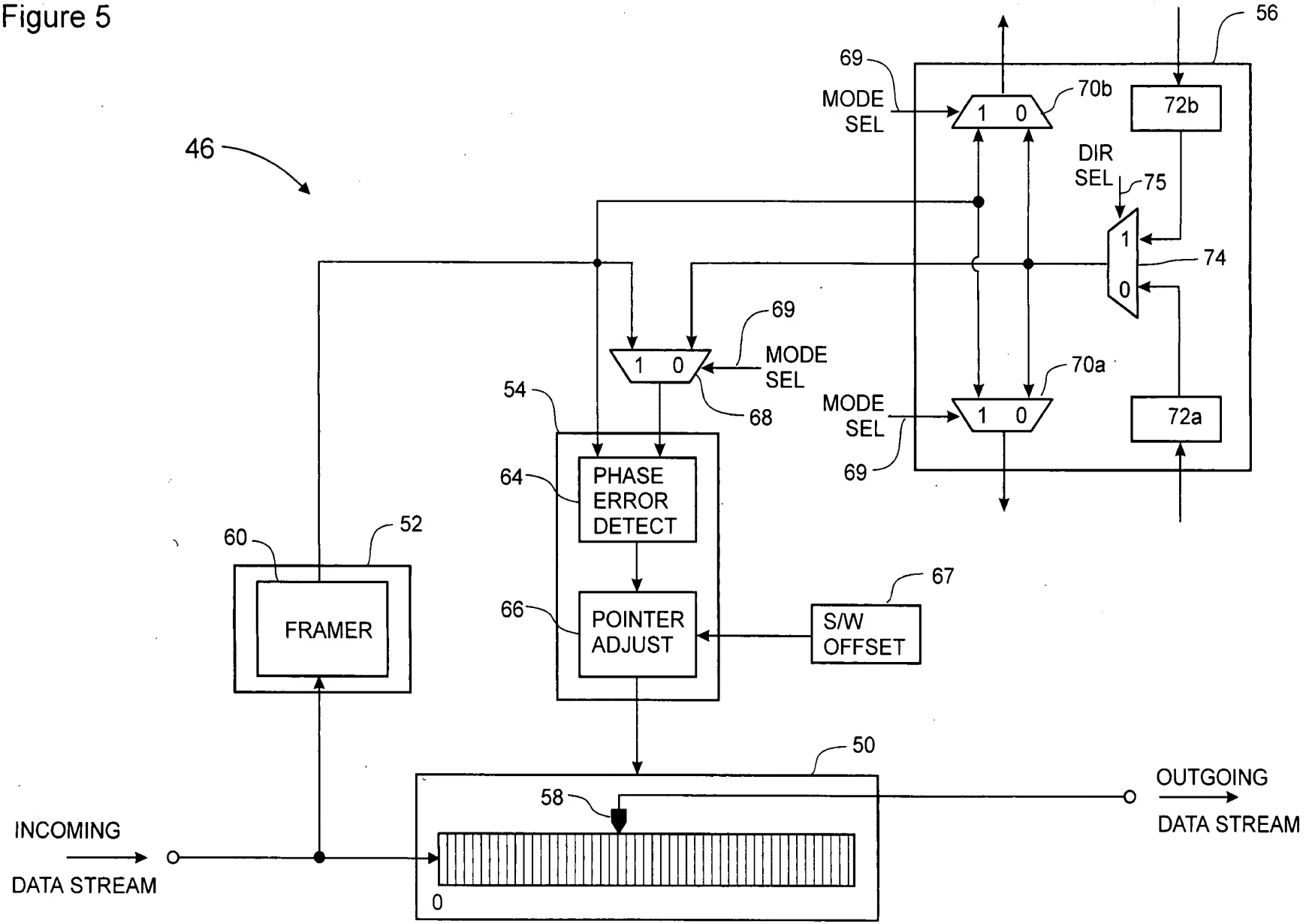
46
56
69
MODE SEL
70b
1 0
72b
DIR SEL
75
1
0
74
69
MODE SEL
1 0
70a
54
MODE SEL
1 0
72a
69
64
PHASE ERROR DETECT
60
52
FRAMER
66
POINTER ADJUST
67
S/W OFFSET
50
58
INCOMING DATA STREAM
OUTGOING DATA STREAM
0

Figure 6a

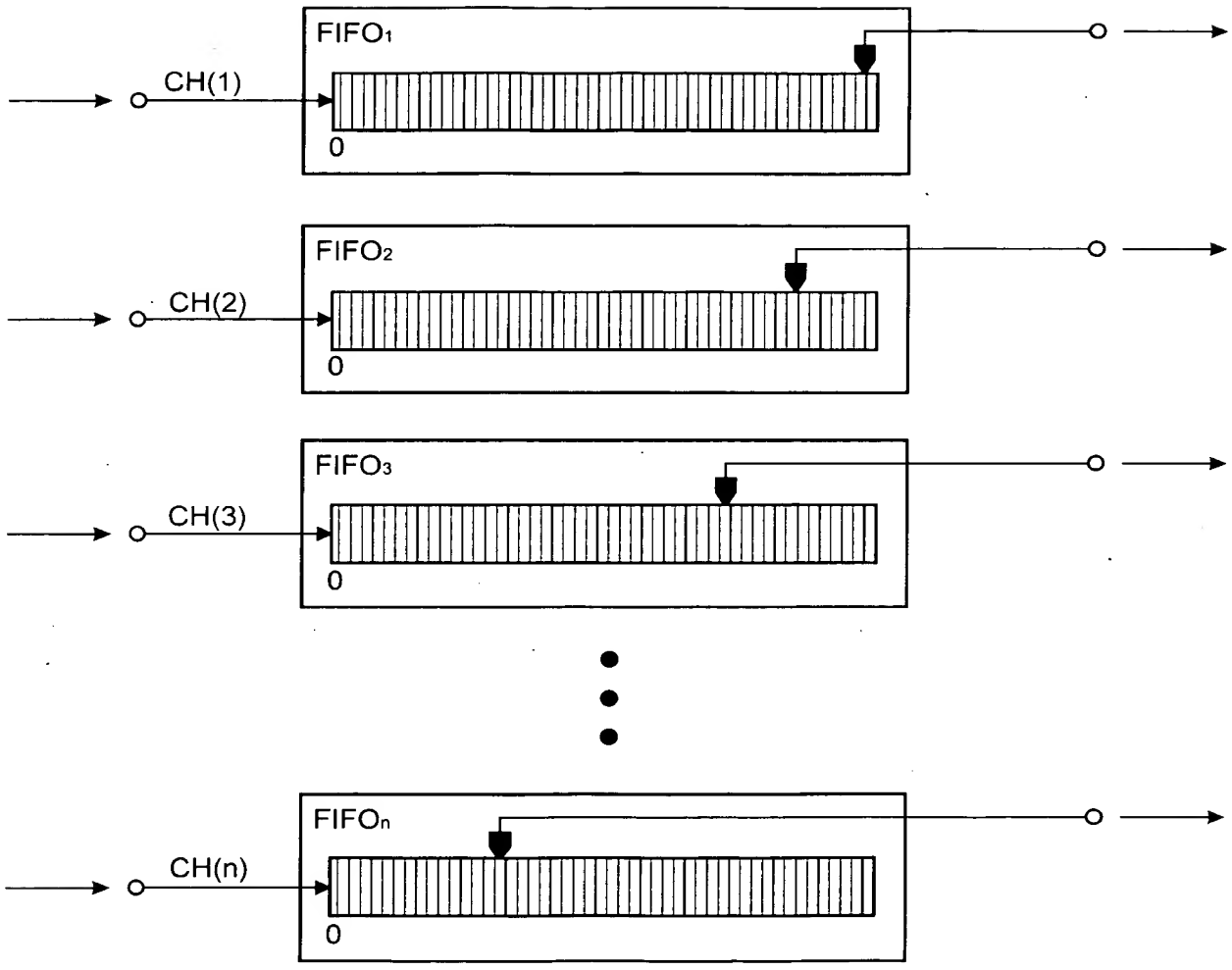

Figure 6b